

Appl. No. 09/833,260

Amdt. Dated March 29, 2004

Reply to Office Action of January 15, 2004

REMARKS

Reconsideration of the application is requested.

Claims 52, 54-56, 58-61, 63-71, and 78-107 are now in the application. Claims 52, 54-56, 58-61, 63-71, and 105-107 are subject to examination and claims 78-104 have been withdrawn from examination. Claims 52, 54, 60, 67, 68, and 105 have been amended. Claims 1-51, 57, and 72-77 have been previously canceled, and claims 53 and 62 are canceled herewith.

In paragraph 3 on page 2 of the above-identified Office Action, the drawings have been objected to under 37 CFR 1.83(a) because they do not show every claimed feature.

More specifically, the Examiner has stated that the drawings do not show an intermediate carrier having a contact connection area and flat conductors and the contact area of the electronic device being oppositely configured as recited in claims 53, 60, 62, 67, and 68.

Claims 53 and 62 have been canceled and claims 60, 67, and 68 have been amended to delete this particular feature and recite only features that are shown in the drawings.

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Accordingly, it is submitted that the basis for the Examiner's objection has been overcome. Therefore, the Examiner is requested to withdraw the objection to the claims.

In paragraph 5 on page 3 of the above-identified Office action, claim 61 has been rejected as failing to comply with the enablement requirement under 35 U.S.C. § 112, first paragraph.

More specifically, the Examiner states that it is not clear from the description in the instant specification "what conditions and parameters are referred to define 'maximum thermal cycling' so that dimensional comparison can be made for the length of the contact element and the respective length difference/increase with respect to centrally located neutral point of the substrate."

In paragraph 7 on page 4 of the above-identified Office Action, claim 61 has been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

In respect of claim 61, the Examiner states that "it is not clear from the description in the specification what conditions and parameters are referred to define 'maximum

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thermal cycling' (recited in the claim) so that a dimensional comparison can be made with respect to the length dimension."

Both of these rejections will be discussed together, because it is believed that applicants comments, which follow, are dispositive of the rejections.

Applicants respectfully submit that claim 61 and the specification of the instant application adequately recite and describe this feature of the present invention and that no further revision of claim 61 is necessary.

The operating temperature range of a particular semiconductor chip is well-known to a person skilled in the art to which the present invention pertains. A typical range for example, may be -40°C to 85°C. The linear thermal expansion of the contact element will depend on the material used for the contact element. Each material chosen to be suitable for a given contact or chip has a known coefficient of thermal expansion.

Therefore, a person skilled in the art can readily determine and calculate the minimum and maximum linear expansion in the contact element from the known maximum and minimum operating temperature and the known thermal expansion coefficient of the contact element material. According to claim 61, the length

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of the contact element is 5% greater than the largest length difference relative to the centrally located neutral point. This determination is within the ability of and routine knowledge to one skilled in the art and does not require special knowledge.

The claimed feature relating to "maximum thermal cycling" is described on page 8, line 13 to page 9, line 3 of the instant specification. As discussed in the previous response, maximum thermal cycling is well-known and understood in the art as the amplitude of lengthening/shortening under maximum rated thermal operating conditions. It is respectfully submitted that one skilled in the art would understand the claimed feature relating to "maximum thermal cycling" when considered in the context of the instant specification and what is known in the industry and prior art. Therefore, no change has been made to claim 61 regarding the limitation.

It is accordingly believed that claim 61 meets the requirements of 35 U.S.C. § 112, first and second paragraphs.

In item 9 on page 5 of the above-identified final Office Action, claims 52-56, 58-71, and 105-107 have been rejected as being unpatentable over Yanof et al. (U.S. Patent No. 5,476,818) (hereinafter "Yanof") in view of Khandros et al.

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(U.S. Patent No. 5,917,707) (hereinafter "Khandros") under 35
U.S.C. § 103(a).

The rejection has been noted and the claims have been amended
in an effort to even more clearly define the invention of the
instant application. Support for the changes is found in the
original claims of the instant application.

Before discussing the prior art in detail, it is believed that
a brief review of the invention as claimed, would be helpful.
Claim 52 calls for, *inter alia*, an electronic device, having:

a substrate being one of a semiconductor chip and a
semiconductor wafer having a surface; and

an electronic circuit having interconnects formed on the
surface of the substrate;

the contact area including a microscopically small contact
element disposed thereon having a base and a substantially
straight part integrally formed at an oblique angle with the
base and extending from the contact area in three dimensions
in a direction deviating from a direction orthogonal to the
surface of the substrate and parallel to the electronic

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circuit on the substrate, the part extending from the contact area being preformed and angularly disposed obliquely

relative to the surface of the substrate in an unstressed condition. (emphasis added)

The present invention enables more reliable electrical connections between a chip and an external intermediate carrier, particularly for testing the circuits of chip-sized packages on the wafer before the singulation and molding processes. The scale of the contact pads and, therefore, the contact elements according to the present claimed invention is completely different relative to the components disclosed by Yanof and Khandros.

The present invention has the advantage over the prior art that, by placing obliquely inclined contact elements onto the chip contact areas, a more accurate positioning of the contact elements on the contact pads is achieved. A more reliable electrical connection to the devices of the chip is therefore produced.

This is a clear and distinct technical advantage over the printed circuit board interposer device of Yanof where flexing and, in particular, lateral sliding of the contact probes of

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the circuit board can easily result in a failure to obtain an electrical contact to the microscopic contact pad on the chip or wafer. Yanof does not address this problem and does not teach or show the present claimed invention.

As acknowledged by the Examiner, Yanof does not show a microscopic contact as recited in the present claims.

Further, Yanof discloses obliquely arranged contact probes attached to a printed board, see Figure 1 for example, while the present claimed invention is directed to the use of obliquely inclined contact elements attached to the contacts pads of a semiconductor chip or wafer.

Independent claims 52 and 105 now recite that the substrate is one of a semiconductor chip or a semiconductor wafer. This feature can be found in previously submitted claim 54, which has been canceled herewith.

Khandros shows resilient extensions for making electrical connections between a semiconductor chip and another circuit board. However, the spring element shown is not a contact element having a base and an extended part integral therewith as recited in the present claims..

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A contact element integrally disposed with the base according to the present invention allows for using particularly thin extended portions in the shape of a pin, which enables such elements to be economically and securely mounted in position on an electronic circuit. Such advantages are not attainable in the prior art.

Khandros (see Fig. 1) shows extensions in the form of pins with a smaller diameter than their base, however, the elongated metal pin 106 is not integrally formed with the base 103 and has to be mounted on the base with means for forming an intimate bond (see column 4, lines 59 et seq.). Khandros does not disclose a straight contact element angularly disposed obliquely relative to the substrate surface as recited in claims 52 and 105. The construction of the contact element according to the present invention (for example, see the bottom paragraph on page 31 of the instant specification) enables contact making by rubbing the free end of the contact element at the opposite contact connection. Khandros does not disclose this feature. In Khandros the element 122 is bent to form a cantilevered configuration (see Fig. 2). The elements shown in Khandros have resiliency, but no ability for lateral movement of the free end. Consequently, the prior art elements do not have a rubbing action which is attained by the

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present claimed invention. Moreover, Khandros does not suggest the possibility of trying to achieve such action.

We disagree that Khandros discloses the use of a microscopically small contact element in a contact area as alleged by the Examiner. Khandros refer to typical contact areas dimensions of 50 to 1250 μm and bonding wire type connections which have a diameter of 12.5 to 75 μm and a length of 250 to 1250 μm . The microscopic contact elements of the instant application are much smaller. Typical contact areas of flip-chips are currently 20 to 40 μm . The disclosure referred to by the Examiner in Khandros is for a "contact pad", not a "microscopically contact element disposed" on a contact area as claimed.

Khandros discloses a wire based contact which may be used in chips and wafers as well as printed circuit boards. The electro-plated contact elements of the present invention have clear advantages over the wire based contacts disclosed in Khandros. The fabrication process of the present invention is faster, because all of the contact elements for an entire wafer are deposited substantially simultaneously, whereas the wire based contacts of Khandros are fabricated one after another.

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Additionally, the contact wires of Khandros are much larger than those of the present invention. The lateral dimensions of the rather long wire connections of Khandros make them unsuitable for use in a wafer level testing system for chip-sized packages. In Khandros, it is apparent from Figs. 23 and 24 and the corresponding description, in particular column 14, line 5, that the lateral dimensions are at least approximately 250 to 375 μm .

A wafer including a plurality of chips designed for chip-sized packages clearly has a higher density of chips on the wafer and a higher density of contact pads on each chip. The distance between the center of adjacent chip contact areas is typically 60 μm . Such a chip and a wafer including these chips requires a more laterally compact contact element to avoid short circuiting between the contacts than the wire bonds of Khandros. This technically advantageous feature and result is provided by the claimed invention.

Also, since the contact elements of the invention can be produced with a diameter of 1 or 2 μm if desired, the present invention also provides a way of increasing the density of contacts on the chip, which is not achievable in the prior art.

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The claimed electronic device of the present invention has significant technical advantages over the devices of Yanof and Khandros. The problems associated with the accurate positioning of flexible contact elements on the densely packed contact pads of chip-sized packages to achieve a reliable electrical connection to an intermediate carrier is a problem not addressed by Yanof or Khandros. Neither reference shows a microscopic contact element on microscopic contact pads of chip-sized packages as recited in the claims of the instant application.

Clearly, the references do not show "a substrate being one of a semiconductor chip and a semiconductor wafer" and "said contact area including a microscopically small contact element disposed thereon having a base and a substantially straight part integrally formed at an oblique angle with said base and extending from said contact area in three dimensions in a direction deviating from a direction orthogonal to said surface of said substrate and parallel to said electronic circuit on said substrate, said part extending from said contact area being preformed and angularly disposed obliquely relative to said surface of said substrate in an unstressed condition" as recited in claim 52 of the instant application. Independent claim 105 contains similar limitations.

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Regarding the Examiner's statements in paragraph B on page 19 of the Office Action relative to claim 105, applicants believe that the claim is patentable over the prior art for the reasons discussed above without regard for the product by process limitations alluded to by the Examiner.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 52 or 105. Claims 52 and 105 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 52 or 105.

Rejoinder of claims 78-104 is requested.

In view of the foregoing, reconsideration and allowance of claims 52, 54-56, 58-61, and 63-71, and 78-107 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in

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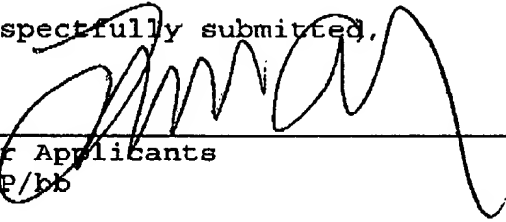
better condition for appeal, without requiring extension of
the field of search.

If an extension of time for this paper is required, petition
for extension is herewith made.

Please charge any other fees that might be due with respect to
Sections 1.16 and 1.17 to the Deposit Account of Lerner and
Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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March 29, 2004

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